Exhibit 14

[redacted]

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Paper 45
Entered: July 30, 2024

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD, MICRON TECHNOLOGY, INC., MICRON SEMICONDUCTOR PRODUCTS, INC., and MICRON TECHNOLOGY TEXAS LLC,[1]
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

IPR2023-00455
Patent 9,858,215 B1

Before GEORGIANNA W. BRADEN, JON M. JURGOVAN, and KEVIN C. TROCK, *Administrative Patent Judges*.

BRADEN, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining All Challenged Claims Unpatentable
Dismissing Petitioner's Motion to Exclude
35 U.S.C. § 318(a)

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[1] Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC filed a motion for joinder and petition in IPR2023-01142 and have been joined as petitioners to this proceeding.

I. INTRODUCTION

In this *inter partes* review, Samsung Electronics Co., Ltd. ("Samsung"), Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC (collectively "Petitioner") challenge the patentability of claims 1–29 of U.S. Patent No. 9,858,215 B1 ("the '215 patent," Ex. 1001), which is assigned to Netlist, Inc. ("Patent Owner").

We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision, issued pursuant to 35 U.S.C. § 318(a), addresses issues and arguments raised during the trial in this *inter partes* review. For the reasons discussed below, we determine Petitioner has proven by a preponderance of the evidence that claims 1–29 of the '215 patent are unpatentable. *See* 35 U.S.C. § 316(e) (2018) ("In an inter partes review instituted under this chapter, the petitioner shall have the burden of proving a proposition of unpatentability by a preponderance of the evidence.").

A. Procedural History

Samsung filed a Petition (Paper 1, "Pet.") challenging claims 1–29 of the '215 patent on the following basis:

Claims Challenged	35 U.S.C. §	References/Basis
1–29	103(a)[2]	Perego,[3] JESD79-2[4]
1–29	103(a)	Perego, JESD79-2, Ellsberry[5]

[2] The Leahy-Smith America Invents Act ("AIA"), Pub. L. No. 112-29, 125 Stat. 284, 287–88 (2011), amended 35 U.S.C. § 103 effective March 16, 2013. Petitioner applies the pre-AIA version of § 103. Pet. 5.
[3] US 7,363,422 B2, issued Apr. 22, 2008 (Ex. 1071).
[4] Joint Electron Devices Engineering Council (JEDEC) DDR2 SDRAM Specification (JESD79-2), September 2003 (Ex. 1064).
[5] US 2006/0277355 A1, published Dec. 7, 2006 (Ex. 1073).

Claims Challenged	35 U.S.C. §	References/Basis
1–29	103(a)	Perego, JESD79-2, Halbert[6]
1–29	103(a)	Perego, JESD79-2, Matsui[7]

Pet. 5. Patent Owner filed a Preliminary Response. Paper 6. With Board authorization (Ex. 3001), Samsung filed a Preliminary Reply (Paper 9) to the Preliminary Response, and Patent Owner filed a Preliminary Sur-reply (Paper 10). Trial was instituted on the asserted grounds of unpatentability. Paper 11 ("Inst. Dec."), 34. After institution, Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC were joined as petitioners to this proceeding based on a petition and a motion for joinder in IPR2023-01142. Paper 26.

During the trial, Patent Owner filed a Response (Paper 22, "PO Resp."), Petitioner filed a Reply (Paper 27, "Pet. Reply"), and Patent Owner filed a Sur-reply (Paper 32, "PO Sur-reply").

Petitioner filed a motion to exclude certain evidence. Paper 35. Patent Owner opposed the motion (Paper 36), and Petitioner filed a reply in support of the motion (Paper 39).

An oral hearing was held on January 11, 2024, a transcript of which appears in the record. Paper 43 ("Tr.").

Petitioner relies on testimony from Andrew Wolfe, Ph.D. Ex. 1003. Patent Owner relies on testimony from Steven Przybylski, Ph.D. Ex. 2024. The parties have entered in the record deposition transcripts of these declarants. Ex. 2033 (Wolfe Deposition); Ex. 1095 (Przybylski Deposition).

[6] US 7,024,518 B2, issued Apr. 4, 2006 (Ex. 1078).
[7] US 2003/0039151 A1, published Feb. 27, 2003 (Ex. 1082).

B. Real Parties in Interest

The identified real parties in interest on the petitioner side are the following: Samsung, Samsung Semiconductor, Inc., Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC. Pet. 1; IPR2023-01142, Paper 2, 1.

Patent Owner identifies itself as the real party in interest. Paper 4, 1.

C. Related Matters

As required by 37 C.F.R. § 42.8(b)(2), the parties identify various related matters. Pet. 1–3; Paper 4 (Patent Owner's Mandatory Notices), 1–3; IPR2023-01142, Paper 2, 1–3. We are issuing concurrently a final decision in IPR2023-00454 involving related U.S. Patent No. 11,093,417 B2 ("the '417 patent").

D. The '215 Patent and Illustrative Claim

The '215 patent relates to memory modules with circuits arranged in ranks of memory. Ex. 1001, code (57). Claim 1 is independent and is reproduced below with Petitioner's claim element identifiers in brackets, which do not impact our analysis. *See* Pet. xiv–xv.

> [1.a.1] A memory module [1.a.2] operable in a computer system to communicate data with a memory controller of the computer system via a memory bus in response to memory commands received from the memory controller, [1.a.3] the memory commands including a first memory command and a subsequent second memory command, the first memory command to cause the memory module to receive or output a first data burst and the second memory command to cause the memory module to receive or output a second data burst, [1.a.4] the memory module comprising:
>
> [1.b] a printed circuit board having a plurality of edge connections configured to be electrically coupled to a

corresponding plurality of contacts of a module slot of the computer system;

[1.c] a register coupled to the printed circuit board and configured to receive and buffer first command and address signals representing the first memory command, and to receive and buffer second command and address signals representing the second memory command;

[1.d.1] a plurality of memory integrated circuits mounted on the printed circuit board and arranged in a plurality of ranks including a first rank and a second rank, the plurality of memory integrated circuits including at least one first memory integrated circuit in the first rank and at least one second memory integrated circuit in the second rank, [1.d.2] wherein the first rank is selected to receive or output the first data burst in response to the first memory command and is not selected to communicate data with the memory controller in response to the second memory command, and [1.d.3] wherein the second rank is selected to receive or output the second data burst in response to the second memory command and is not selected to communicate data with the memory controller in response to the first memory command;

[1.e] a buffer coupled between the at least one first memory integrated circuit and the memory bus, and between the at least one second memory integrated circuit and the memory bus; and

[1.f.1] logic coupled to the buffer and configured to respond to the first memory command by providing first control signals to the buffer to enable communication of the first data burst between the at least one first memory integrated circuit and the memory controller through the buffer, [1.f.2] wherein the logic is further configured to respond to the second memory command by providing second control signals to the buffer to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer, the second control signals being different from the first control signals.

Ex. 1001, 37:13–62.

II. ANALYSIS

A. Principles of Law

"In an IPR, the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable." *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify "with particularity . . . the evidence that supports the grounds for the challenge to each claim")). This burden of persuasion never shifts to Patent Owner. *See Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015) (discussing the burden of proof in *inter partes* review).

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) any secondary considerations, if in evidence. *Graham v. John Deere Co. of Kan. City*, 383 U.S. 1, 17–18 (1966).

B. Level of Ordinary Skill in the Art

Petitioner argues that a person of ordinary skill in the art "would have had an advanced degree in electrical or computer engineering and at least two years working in the field, or a bachelor's degree in such engineering disciplines and at least three years working in the field" and that

"[a]dditional training can substitute for educational or research experience, and vice versa." Pet. 9 (citing Ex. 1003 ¶ 48); *see* Pet. Reply 1. Petitioner argues that a person of ordinary skill in the art "would have been familiar with various standards of the day including the JEDEC [(Joint Electron Devices Engineering Council)] industry standards, and knowledgeable about the design and operation of standardized DRAM and SDRAM[8] memory devices and memory modules and how they interacted with the memory controller of a computer system." Pet. 9 (citing Ex. 1003 ¶ 48). Petitioner identifies other items within the ordinarily-skilled artisan's knowledge base, including "the structure and operation of circuitry used to access and control computer memories, including sophisticated circuits such as ASICs (Application-Specific Integrated Circuits) and CPLDs (Complex Programmable Logic Devices) and more low-level circuits such as tri-state buffers, flip flops and registers" and

> JEDEC DDR and DDR2 SDRAM standards used to standardize the functioning of memory devices, and the JEDEC 21-C standard used to standardize different possibilities for the physical layout of memory devices on a module as well as different possibilities for density and organization of the memory devices to achieve a given memory capacity.

Id. at 9–10 (citing Ex. 1003 ¶¶ 48–50; Ex. 1001, 5:63–6:11, 21:7–22:7, 34:26–33; Exs. 1060, 1062, 1064, 1066).

[8] DRAM (Dynamic Random-Access Memory) operates asynchronously with slower speeds and higher latency, while SDRAM (Synchronous Dynamic Random-Access Memory) synchronizes with the system clock for faster, more efficient data transfer. Ex. 1071, 4:1–12.

Patent Owner "applies the skill level proposed by Petitioner." PO Resp. 8. According to Patent Owner, "no aspect of this IPR . . . turns on this dispute." PO Sur-reply 4.

We accept the uncontested assessment offered by Petitioner, except that we delete the qualifier "at least" to eliminate vagueness as to the amount of experience. The qualifier expands the range indefinitely without an upper bound, and thus precludes a meaningful indication of the level of ordinary skill in the art.

C. Claim Construction

We interpret claim terms using "the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b)." 37 C.F.R. § 42.100(b). Independent claim 1 recites memory devices arranged in ranks. Petitioner argues that a "rank" is "an independent set of one or more memory devices on a memory module that act together in response to command signals, including chip-select signals, to read or write the full bit-width of the memory module." Pet. 27–28 (citing Ex. 1003 ¶ 126); Pet. Reply 1–2.

Patent Owner disagrees that a rank can be a single memory device, but states that "the Board need not resolve that dispute to address the parties' arguments regarding the challenged claims" because Patent Owner "applies Petitioner's proposed construction" "[s]olely for purposes of responding to this Petition." PO Resp. 8–9; PO Sur-reply 4–5. Patent Owner also apprises us of a construction of "rank" from related district court litigation. PO Resp. 8 (citing Ex. 2030, 12–15). Our Rules provide that "[a]ny prior claim construction determination concerning a term of the claim in a civil action, or a proceeding before the International Trade Commission, that is timely

made of record in the inter partes review proceeding will be considered." 37 C.F.R. § 42.100(b). We have considered the district court's construction, and we note that, like Petitioner's proposed construction, it provides that a rank can be one memory device. *See* Ex. 2030, 14 ("Accordingly, the Court concludes a 'rank' can include a single memory device.").

For our patentability analysis, we apply the construction of "rank" used by both parties (i.e., the construction proposed by Petitioner), and we need not engage in any further claim construction because there are no claim construction disputes that bear on the issues before us. *See Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) ("The Board is required to construe 'only those terms . . . that are in controversy, and only to the extent necessary to resolve the controversy.'" (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

D. Alleged Obviousness of Claims 1–29 in View of Perego and JESD79-2

Petitioner asserts that claims 1–29 are unpatentable because they would have been obvious to a person of ordinary skill in the art at the critical time in view of the combined teachings of Perego and JESD79-2. Pet. 5, 30–112. Patent Owner opposes. PO Resp. 19–33; PO Sur-reply 6–19. For reasons that follow, we determine Petitioner has shown by a preponderance of the evidence that the challenged claims are unpatentable under 35 U.S.C. § 103(a).

1. Overview of the Asserted Prior Art

a. Perego (Ex. 1071)

Perego pertains to memory systems and discloses a memory module with a configurable width buffer device. Ex. 1071, code (57). One embodiment of Perego is shown in Figure 3C, reproduced below.

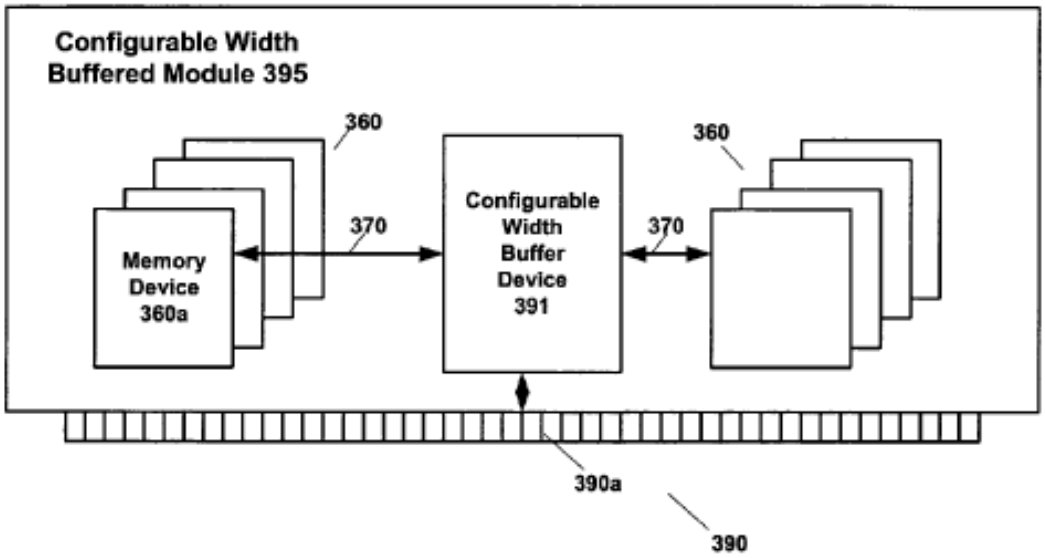

Fig. 3C

Perego's Figure 3C, above, is a block diagram illustrating a "memory module that includes a configurable width buffer device" having configurable width buffer device 391 (not shown) that is connected on the bottom to interface connections 390a in connector 390 and that is connected on the sides to memory devices 360 via channels 370. Ex. 1071, 2:43–45, 7:30–39.

Another embodiment of Perego is shown in Figure 5B, reproduced below.

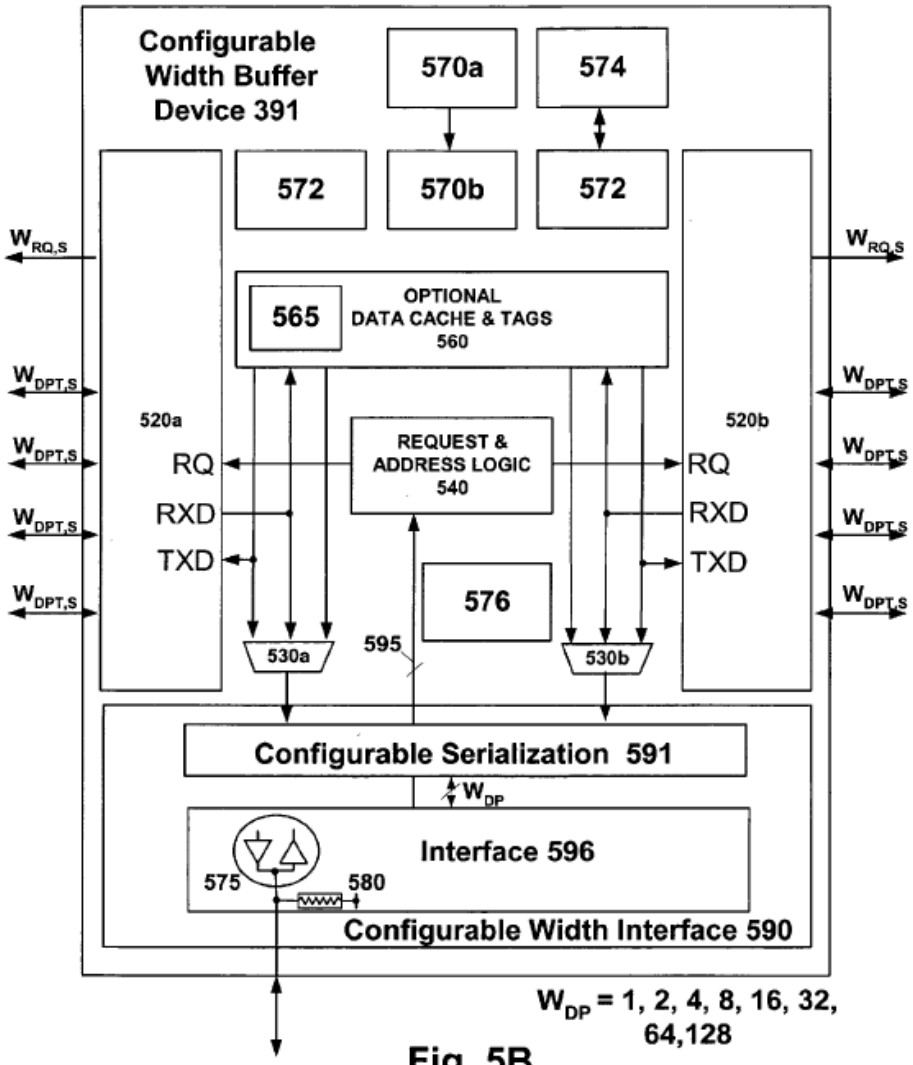

Fig. 5B

Perego's Figure 5B, above, is block diagram illustrating a configurable width buffer device 391, and we discuss this figure and the accompanying disclosure in detail in our analysis below. *See* Ex. 1071, 2:51–53, 13:6–8 ("FIG. 5B illustrates a configurable width buffer device 391 as seen in FIG. 3C in an embodiment of the present invention."). Perego also discloses that Double Data Rate 2 ("DDR2") memory devices can be used on its memory modules. *Id.* at 10:56–59.

b. JESD79-2 (Ex. 1064)

JESD79-2 is a JEDEC standard for DDR2 memory devices. Ex. 1064. It was published in September 2003 and provides industry standards for the programming and operating modes of DDR2 SDRAM. *Id.* at 12. The standard specifically addresses additive latency (AL) in the DDR2 SDRAM Extended Mode Register Set (EMRS). *Id.* at 14. Per the standard, the Read Latency (RL) is controlled by the sum of the additive latency (AL) and the CAS latency (CL). *Id.* at 24. Therefore, according to JESD79-2, if a user chooses to issue a R/W (read/write) command before the Internal RAS-CAS-Delay Time (tRCDmin), then AL (greater than 0) must be written into the EMRS(1). *Id.* The Write Latency (WL) is always defined as RL - 1 (read latency -1) where read latency is defined as the sum of additive latency plus CAS latency (RL=AL+CL). *Id.* Read or Write operations using AL allow seamless bursts (refer to seamless operation timing diagram examples in Read burst and Write burst section). *Id.* JESD79-2 discloses that the RL is equal to an additive latency (AL) plus CAS latency (CL), where CL is defined by the Mode Register Set (MRS), similar to the existing SDR and DDR SDRAMs, while AL is defined by the Extended Mode Register Set (1) (EMRS(1)). *Id.* at 26.

2. Analysis of Claim 1

Claim 1 recites a memory module having various components that are configured or configurable to operate in a particular manner, which we address in more detail below. To address claim 1, Petitioner relies on Perego's memory module disclosures in combination with JESD79-2's disclosures of DDR2 memory operations. Pet. 29–80. Patent Owner disputes Petitioner's contentions and argues that an ordinarily skilled artisan

at the critical time would not have had reason to alter Perego's memory modules as Petitioner suggests. PO Resp. 19.

a) Preamble (1.a.1)

The preamble of claim 1 recites the following:

> [1.a.1] A memory module [1.a.2] operable in a computer system to communicate data with a memory controller of the computer system via a memory bus in response to memory commands received from the memory controller, [1.a.3] the memory commands including a first memory command and a subsequent second memory command, the first memory command to cause the memory module to receive or output a first data burst and the second memory command to cause the memory module to receive or output a second data burst, [1.a.4] the memory module comprising.

Petitioner argues that Perego's Figures 3B, 3C, 4A, 4B, and 4C show memory modules that communicate data with a memory controller of a computer system via a bus. Pet. 35–46. Perego's Figure 4A is reproduced below.

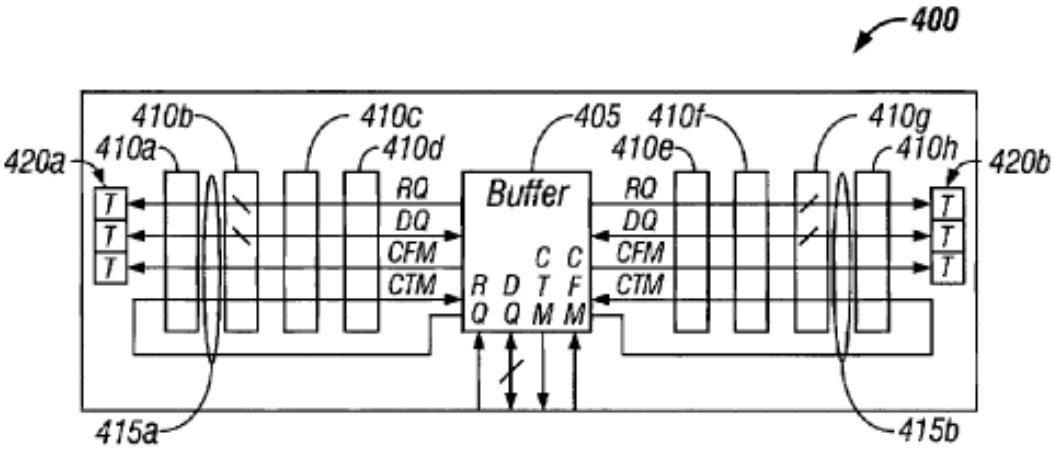

FIG. 4A

Perego's Figure 4A, above, is a diagram showing memory module 400 with buffer 405 connected to memory devices 410a–h over a pair of channels 415a and 415b. Ex. 1071, 9:26–33.

For the recited memory commands, Petitioner cites Perego's disclosure of storing and retrieving data in response to commands, and Petitioner argues that a person of ordinary skill in the art would "have understood from their own knowledge of JEDEC standards, including JESD79-2, the specific ways to issue read and write commands to Perego's DDR2 memory devices." Pet. 42 (citing Ex. 1064, 6, 24–33, 49; Ex. 1003 ¶ 227).

Petitioner also argues that Perego discloses the recited "operable to communicate data with a memory controller" limitation because Perego's memory bus (link 320a) can have a data width of W_{DP} = 16, 32, 64, or 128 that pass information on the DQ data lines through one or more busses. Pet. 37–42 (citing Ex. 1071, Figs. 4A–4B, Figs. 5A–5B, 3:41–47, 5:6–24, 11:8–12, 14:16–51; Ex. 1003 ¶¶ 220–224). According to Petitioner, an ordinarily skilled artisan at the critical time "would have understood that a data width of W_{DP} = 64 corresponds to the 64-bit data width of a JEDEC-compliant registered DIMM module." *Id.* at 39 (citing Ex. 1062, 5; Ex. 1003 ¶ 224).

Petitioner then argues Perego teaches the required memory command because "Perego discloses using DDR SDRAM devices that store or retrieve data in response to 'a write or read command.'" Pet. 42 (citing Ex. 1071, 3:64–4:12, 8:1–4, 10:56–58). Petitioner asserts that a person of ordinary skill in the art would have understood from JESD79-2 that a first write or read command can be followed by a "*subsequent*" second write or read command. *Id.* at 42–43 (citing Ex. 1064, 24–33, Fig. 26; Ex. 1003 ¶¶ 232, 237).

Patent Owner does not dispute that the combination of Perego and JESD79-2 teaches the subject matter recited in the preamble, but does dispute Petitioner's contentions regarding implementing Perego's module as a JEDEC-compliant DIMM. PO Resp. 21–24 (citing Ex. 2024 ¶¶ 132–134). Based on Petitioner's persuasive contentions and evidence, summarized and cited above, we find that the combination of Perego and JESD79-2 teaches the subject matter recited in the preamble. In view of this finding, we need not decide whether the preamble is limiting.

We address the parties' dispute about a JEDEC-compliant module below in our discussion of the "logic coupled to the buffer and configured to respond to the first memory command by providing first control signals" subject matter of claim 1.

b) Printed circuit board (1.b)

Claim 1 recites "a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system." Petitioner argues that Perego's disclosure of including memory modules on printed circuit boards (PCBs) with connectors (such as connectors 390a in Figure 3C) teaches this subject matter. Pet. 46–48 (citing Ex. 1071, 5:56–6:11, 7:39–41, Figs. 3B, 3C; Ex. 1003 ¶¶ 243–248); *see, e.g.*, Ex. 1071, 5:60–62 (disclosing that "memory subsystems are incorporated onto individual substrates (e.g., PCBs)").

Patent Owner does not dispute this specific contention. *See generally* PO Resp. Rather, Patent Owner disputes Petitioner's contentions about implementing Perego's module as a JEDEC-compliant DIMM, and we address this dispute below in our discussion of the "logic coupled to the

buffer and configured to respond to the first memory command by providing first control signals" subject matter of claim 1. Nonetheless, the burden remains on Petitioner to demonstrate unpatentability. *See Dynamic Drinkware*, 800 F.3d at 1378.

Based on the entire trial record, we agree with Petitioner's analysis and we credit Dr. Wolfe's testimony supporting Petitioner's position. Accordingly, we find that Perego discloses limitation 1.b.

c) Register (1.c)

Claim 1 recites "a register coupled to the printed circuit board and configured to receive and buffer first command and address signals representing the first memory command, and to receive and buffer second command and address signals representing the second memory command."

Petitioner contends that Perego's buffer device 350 coupled to the printed circuit board teaches this subject matter. Pet. 48–54. Petitioner argues that Perego teaches this subject matter by its disclosure of buffer devices in the memories receiving control and address information for memory operations. *Id.* (citing Ex. 1071, 5:6–15, 6:12–33, 8:1–4, 9:50–60, 10:56–59, 11:8–12, 13:54–59, Figs. 3B, 4A, 4B, 5A, 5B, 5C; Ex. 1062, 12; Ex. 1064, 26, 29, 49; Ex. 1003 ¶¶ 251–253, 256–258). Petitioner further argues that a person of ordinary skill in the art "would have understood that '*command and address signals*' representing a respective memory command would be received from the memory controller because the receiving of command and address information is naturally associated with a memory command." *Id.* at 53–54 (citing Ex. 1003 ¶¶ 256–258). Petitioner also contends that JESD79-2 discloses that "read and write commands include both address signals (e.g., BA0–BA2, A0–A15) and control signals (e.g., CS

chip select, RAS, CAS, WE)." Pet. 48 (citing Ex. 1064, 6, 49; Ex. 1003 ¶ 238).

Patent Owner does not dispute this specific contention. *See generally* PO Resp. Rather, Patent Owner disputes Petitioner's contentions about implementing Perego's module as a JEDEC-compliant DIMM, and we address this dispute below in our discussion of the "logic coupled to the buffer and configured to respond to the first memory command by providing first control signals" subject matter of claim 1. Nonetheless, the burden remains on Petitioner to demonstrate unpatentability. *See Dynamic Drinkware*, 800 F.3d at 1378.

Based on the entire trial record, we agree with Petitioner's analysis and we credit Dr. Wolfe's testimony supporting Petitioner's position. Accordingly, we find that Perego discloses limitation 1.c.

d) Ranks (1.d) – Memory Integrated Circuits (1.d.1)

Claim 1 recites:

> a plurality of memory integrated circuits mounted on the printed circuit board and arranged in a plurality of ranks including a first rank and a second rank, the plurality of memory integrated circuits including at least one first memory integrated circuit in the first rank and at least one second memory integrated circuit in the second rank.

Petitioner argues that Perego teaches memory circuits arranged in ranks by disclosing groups of memory devices that are accessed together in a memory operation. Pet. 54–62 (citing Ex. 1071, 2:4–6, 3:62–4:3, 4:19–22, 6:12–24, 8:1–4, 10:56–58, 14:10–40, 17:22–28, 21:16–20, Figs. 3C, 4A, 4B, 4C, 5A, 5B; Ex. 1003 ¶¶ 261–282). For example, Perego discloses "grouping memory devices into multiple independent target subsets (i.e. more independent banks)." Ex. 1071, 15:37–45, *quoted in* Pet. 56.

Petitioner provides the version of Perego's Figure 3C below.

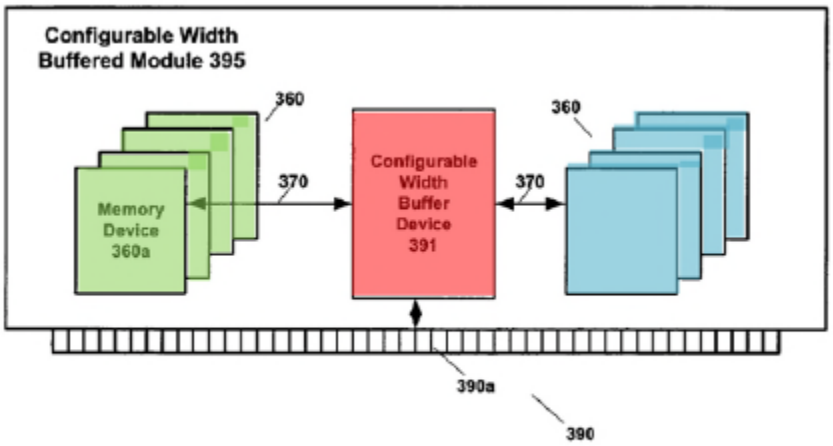

Fig. 3C

Pet. 54, 60. Perego's Figure 3C above is a block diagram of configurable width buffered module 395 having configurable width buffer device 391 (shaded red) connected on each side via channels 370 to multiple memory devices 360 (shaded green on the left and blue on the right). Ex. 1071, 2:43–45, 7:30–34; Pet. 54, 60. Noting Perego's disclosure that "one or more of channels 370" can be used in an operation (Ex. 1071, 6:12–24), Petitioner argues that, "when Perego's buffer device has two channels, and each channel is connected to one rank, Perego's module includes two ranks of memory devices (green and blue . . .)." Pet. 59–60 (citing Ex. 1003 ¶ 269).

Petitioner also points to Perego's disclosure of a configurable width buffer having interfaces that may be programmed to have a 64-bit width by connecting to multiple devices having a total width of 64 bits. Pet. 57–58 (citing Ex. 1071, 14:10–15, Figs. 5A, 5B). Petitioner argues that "Perego teaches that the data width accessed in a memory transaction (W_A), and the data width of the buffer interfacing with the memory controller (W_{DP}), can both be the same (e.g., both 64 bits), such that the ratio $W_A/W_{DP} = 1{:}1$." *Id.* at 59 (citing Ex. 1071, 14:16–40, 17:22–28, Fig. 5C; Ex. 1003 ¶ 267).

According to Petitioner, a person of ordinary skill in the art "would understand that W_A refers to the bit-width of each '*rank*' of memory devices (e.g., 64 bits can be read or written at a time) when only '***one***' of the 'one or more channels 370' . . . is used for a read or write operation." *Id.* (citing Ex. 1071, 6:12–24, 14:23–27, Fig. 3C; Ex. 1003 ¶¶ 268–269).

In addition to its argument that Perego discloses one rank per channel, Petitioner also argues that the memory devices connected to two channels may be considered one rank when the devices on the channels act together. Pet. 60–62 (citing Ex. 1071, 21:16–20, Figs. 4B, 4C). For example, Perego discloses, with reference to Figure 4B, that "[a]ny number of channels 415a-415d, for example, two channels 415c and 415d *may transfer information simultaneously* and the memory devices on the other two channels 415a and 415b remain in a ready or standby state until called upon to perform memory access operations." Ex. 1071, 21:16–20 (emphasis added).

Petitioner contends that "it would have been obvious to a [person of ordinary skill in the art] to arrange Perego's DDR memory devices into '*ranks*,' and a [person of ordinary skill in the art] would have been motivated to do so, in light of the JEDEC standards." Pet. 62 (citing Ex. 1064, 6; Ex. 1062, 13, 27–30; Ex. 1003 ¶¶ 273–275). Petitioner relies on JESD79-2's disclosure of chip select signals for ranks. *Id.* (citing Ex. 1064, 6; Ex. 1003 ¶¶ 273–275; Ex. 1062, 13).

Patent Owner argues that Perego does not teach "ranks" of memory devices. PO Resp. 33–35. According to Patent Owner, even applying Petitioner's proposed claim construction of "rank," Perego does not disclose such "ranks," because Petitioner's construction requires chip-select signals. *Id.* at 33 (citing Ex. 2024 ¶¶ 157–166). According to Patent Owner, a person

of ordinary skill in the art would have understood the memories depicted in Perego's Figures 4A-4C to be Direct RDRAM embodiments, which do not receive chip-select signals. *Id.* (citing Ex. 2024 ¶¶ 159, 162; Ex. 1071, 10:54–56). Patent Owner then argues that "Rambus memory devices are incompatible with the concept of ranks because they are each accessed individually and thus do not 'act together' as proposed by Petitioner." *Id.* (citing Ex. 2001, 23).

We disagree with Patent Owner. Rather, upon review of the entirety of the record, we find that Perego discloses that each of the interfaces in configurable width buffer device 391 of Figure 5B, on which Petitioner relies (Pet. 57–59), may connect to multiple devices, resulting in a width of 64 bits. Ex. 1071, 14:12–15; *see* Pet. 57–58 (discussing this disclosure). In particular, Perego discloses that "interfaces 520a and 520b may be programmed to connect to 16'x4' width memory devices, 8'x8' width memory devices or 4'x16' width memory devices." Ex. 1071, 14:12–15; *see* Pet. 57–58 (discussing this disclosure). Perego explains that the "maximum memory device access width" is "the largest number of bits that can be accessed in a *single memory device transfer operation* to or from configurable width buffer device 391." Ex. 1071, 14:23–27 (emphasis added). Perego also discloses that a memory operation may occur on one of channels 370. *Id.* at 6:12–24; *see* Pet. 59 (discussing this disclosure). On the entirety of the record, in view of Perego's disclosures, we find that, when there are multiple memory devices that account for the memory device access width (e.g., 64 bits), then those devices "act together" as in Petitioner's proposed construction. *See* Pet. 27–28. Furthermore, Perego discloses a serialization ratio of 1:1, meaning that the memory device access

width (W_A) and the configured buffer device interface width (W_{DP}) are the same. Ex. 1071, 14:32–40, 17:22–28. In such a configuration, each rank would match the full bit-width of the memory module as in Petitioner's proposed construction. *See* Pet. 27–28.

Additionally, we find that Petitioner relies on JESD79-2 for its disclosure of chip select signals (*see* Pet. 62), and, as discussed in detail below, we find that a person of ordinary skill in the art would have had reason to combine the teachings of Perego and JESD79-2 given Perego's express disclosure of using DDR2, for which the industry specification is JESD79-2.

Accordingly, based on the entirety of the trial record, we find that Perego discloses limitation 1.d.1.

e) Receive or Output Data in Response to Memory Commands (1.d.2), (1.d.3)

Claim 1 recites:

> wherein the first rank is selected to receive or output the first data burst in response to the first memory command and is not selected to communicate data with the memory controller in response to the second memory command, and
>
> wherein the second rank is selected to receive or output the second data burst in response to the second memory command and is not selected to communicate data with the memory controller in response to the first memory command.

Petitioner argues that Perego teaches this subject matter because it discloses reading from or writing to a target subset of devices (rank) and also discloses that some devices remain in a standby state such that they are not selected as the target devices. Pet. 63–68 (citing Ex. 1071, 6:21–22, 11:56–61, 15:31–45, 21:16–20, Figs. 3C, 4A, 4B, 4C, 5A, 5B; Ex. 1003 ¶¶ 283–303). For example, Perego discloses "grouping memory devices into

multiple independent target subsets (i.e. more independent banks)" and "rout[ing] data from an appropriate source (i.e. target a subset of channels, internal data, cache or write buffer)." Ex. 1071, 15:42–45, 11:56–61. Perego also discloses that "two channels 415c and 415d may transfer information simultaneously and the memory devices on the other two channels 415a and 415b remain in a ready or standby state until called upon to perform memory access operations." *Id.* at 21:16–20.

Apart from its arguments about "ranks," discussed in the preceding section, Patent Owner does not dispute Petitioner's contentions for this limitation. Nonetheless, the burden remains on Petitioner to demonstrate unpatentability. *See Dynamic Drinkware*, 800 F.3d at 1378.

Based on the entire trial record, we agree with Petitioner's analysis and we credit Dr. Wolfe's testimony supporting Petitioner's position. Accordingly, we find that Perego discloses limitations 1.d.2 and 1.d.3.

f) Buffer (1.e)

Claim 1 recites "a buffer coupled between the at least one first memory integrated circuit and the memory bus, and between the at least one second memory integrated circuit and the memory bus; and."

Petitioner argues that Perego's buffer device "isolat[es] the memory controller from signals interfacing with the memory devices" and, therefore, is a buffer as recited in claim 1. Pet. 73–76 (citing Ex. 1071, 4:38–42, 6:12–15, 7:30–34, 10:59–67, 11:1–7, 13:6–10, 13:18–24, 14:65–15:2, 17:61–63, 18:65–19:3, Figs. 5A, 5B, 5C; Ex. 1003 ¶¶ 304–311).

Patent Owner does not dispute Petitioner's contentions for this limitation. Nonetheless, the burden remains on Petitioner to demonstrate unpatentability. *See Dynamic Drinkware*, 800 F.3d at 1378.

Based on the entire trial record, we agree with Petitioner's analysis and we credit Dr. Wolfe's testimony supporting Petitioner's position. Accordingly, we find that Perego discloses limitation 1.e.

g) Logic (1.f.1), (1.f.2)

Claim 1 recites:

> logic coupled to the buffer and configured to respond to the first memory command by providing first control signals to the buffer to enable communication of the first data bust between the at least one first memory integrated circuit and the memory controller through the buffer,
>
> wherein the logic is further configured to respond to the second memory command by providing second control signals to the buffer to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer, the second control signals being different from the first control signals.

(1) Petitioner's Arguments

Petitioner argues that Perego teaches this subject matter because it discloses that different target memory subsets (ranks) on different channels are selected for different operations such that control signals activate only the channel over which the operation is performed. Pet. 76–80 (citing Ex. 1071, 6:15–25, 11:56–61, 12:9–12, 13:54–59, 21:16–20, Figs. 5A, 5B; Ex. 1003 ¶¶ 312–324). Petitioner further argues that a person of ordinary skill in the art

> would have understood that, because interfaces 520a/b, 510, and 590 include transceivers (e.g., 575), and because multiplexer/demultiplexer circuit 597 (e.g., in 591) contains "multiplexing logic and demultiplexing logic," Perego's buffer device includes logic that sends "*control signals*" to the transceivers, multiplexing/demultiplexing circuits, and to the input and output latches to selectively activate those circuit

> elements of the buffer according to the targeted rank and direction of the read and write operations.

Id. at 80 (citing Ex. 1071, 14:62–15:6, 15:34–40, 17:41–44, 17:61–62, Figs. 5A, 5B; Ex. 1003 ¶¶ 318–319).

Petitioner also contends that JESD79-2 discloses that read and write commands include both address signals (e.g., BA0–BA2, A0–A15) and control signals (e.g., CS chip select, RAS, CAS, WE). Pet. 59 (citing Ex. 1003 ¶¶ 268–269). Petitioner argues that it "would have been obvious to a [person of ordinary skill in the art] in light of JESD79-2 and knowledge of the JEDEC standards that the memory controller would provide multiple chip-select signals to the memory module" where the signals correspond to multiple ranks of memory devices and where one of the signals is active to select the target rank and the other signals are inactive. *Id.* at 57–58 (citing Ex. 1062, 6; Ex. 1066, 6–7; Ex. 1003 ¶¶ 251–252); *see also Id.* at 52–54 (explaining that chip select signal (CS) is active low).

Petitioner then contends that Perego is consistent with JESD79-2's disclosure of selecting particular groups of memory devices because "Perego discloses that its module includes multiple sets of memory devices (e.g., 'ranks,' . . .), each of which can be a target of a memory read or write command, and each of which acts together in response to a memory read or write command." Pet. 54–57 (citing Ex. 1071, 6:12–24, 15:37–45, Figs. 3C, 4A, 4B, 4C; Ex. 1003 ¶¶ 249–250).

According to Petitioner, a person of ordinary skill in the art would have had reason to combine the teachings of Perego and JESD79-2 because Perego discloses that its memory modules can use DDR2 memory devices and "the JEDEC standard for DDR2 memory devices is JESD79-2." Pet. 32 (citing Ex. 1071, 3:62–4:12, 8:1–4, 10:54–67; Ex. 1064); *see also id.* at 30–

33 (further explaining rationale to combine). Petitioner then asserts that a person of ordinary skill in the art would have been motivated to make Perego's memory modules JEDEC-compliant "to allow these modules to be used in JEDEC-compliant memory systems, such as those using DIMM modules of the format described by JESD21-C." *Id.* at 33 (citing Ex. 1003 ¶ 185).

Petitioner further argues that a person of ordinary skill in the art would have understood that Perego's buffer device 'register[s]' address and control signals similar to a JEDEC-compliant conventional registered DIMM. Pet. 49–50 (citing Ex. 1071, 6:15–30, 13:54–59, Fig. 5C; Ex. 1062, 12; Ex. 1003 ¶¶ 239–240).

(2) Patent Owner's Arguments

Patent Owner argues that a JEDEC-compliant module that receives chip select signals "is fundamentally at odds with" Perego's architecture, which Patent Owner asserts is "a Rambus-style point-to-point topology." PO Resp. 9 (citing Ex. 1071, code (57), 4:38–45, 5:35–55, 8:10–17, 8:20–26), 23–24. According to Patent Owner, "Perego discloses Rambus-style modules that employ a point-to-point architecture and configurable bit-width interfaces that are fundamentally different than the conventional memory bus required by JEDEC module standards and do not include chip-select lines or otherwise convey chip-select signals." *Id.* at 1. Patent Owner further argues that "Perego repeatedly and consistently emphasizes the benefits of its point-to-point architecture over a conventional JEDEC-style bus." *Id.* at 9–10 (citing Ex. 1071, 3:47–56, 4:65–5:1, 5:6–15, 5:32–55, 6:15–19, 13:49–59, 21:46–50, Figs. 3A/3B, Fig. 5A). Patent Owner explains that "in contrast to a conventional registered DIMM ('RDIMM'), in

Perego's architecture, control/address information is transmitted to the module via packets and multiplexed with data in order to be transmitted via the point-to-point links." *Id.* at 10 (citing Ex. 1071, 13:49–59).

Patent Owner's declarant, Dr. Przybylski, testifies that "Perego specifically refers to a dynamic point-to-point topology to connect the memory controller to the memory subsystem/module" and that a person of ordinary skill in the art, "being familiar with the Rambus XDR architecture, would recognize this terminology as being specific to the XDR architecture." Ex. 2024 ¶ 99 (citing Ex. 1071, 3:41–47, 5:32–35, 6:57–7:29, 8:1–9; Ex. 2009, 10–12, 15, 17).

The assignee of the Perego patent is Rambus, Inc. (Ex. 1071, code (73)), and there is no dispute that Perego discloses features that are consistent with Rambus's point-to-point architecture. And, it may be true that a person of ordinary skill in the art would have understood Perego's point-to-point terminology to refer to the Rambus XDR architecture, and Perego mentions Rambus XDR memory devices. *Id.* at 8:1–9. But, as explained below, Perego's disclosures are not limited to that architecture. For example, Perego discloses that "one or more busses *or* a plurality of point-to-point links may be used to couple one or more buffer devices to a master (e.g., a controller or microprocessor device)" and that a "dynamic point-to-point link topology *or* any combination of point-to-point links or busses may be used to interface the master device and a corresponding buffer device." *Id.* at 3:41–47 (emphasis added). Thus, Perego discloses that a bus, as an alternative to point-to-point links, may be used to connect the module to the memory controller.

Dr. Przybylski further explains that

> Perego's memory system (300 or 305) is built with a plurality of point-to-point buses (320) connecting a memory controller (310) with memory subsystems (330). Ex. 1071, Figure 3A, 3B, 4:63–5:15. These memory subsystems can be inserted into sockets (380) and in these embodiments comprise modules (340, 400). Though several embodiments of buses 320 are disclosed they are all point-to-point with one end connected to the memory controller and the other to the memory subsystem. Ex. 1071, Figures 3A, 3B, 6A, 6B, 7, 8A, 8B, 8C, 4:63–5:15, 20:48–64, 20:65–21:3, 21:39–22:9. The point to point links are used to convey read and write data, and address and control information can be multiplexed with data or be transported on their own buses. Ex. 1071, Figures 5A, 5B, 5:16–31, 8:10–19, 13:49–59.

Ex. 2024 ¶ 98. Here, Dr. Przybylski refers to the elements labeled 320 in Perego as "point-to-point buses," but Perego does not use this terminology. Rather, Perego refers to every instance of element 320 as "point-to-point link[s]." *See* Ex. 1071, 4:66–67, 5:14–15, 5:56, 5:63–64, 6:11, 6:17, 6:23–24, 7:1, 7:3, 7:8–9, 8:20, 8:42, 8:48–49, 8:67, 9:8, 9:48, 11:9, 11:12, 11:22, 11:27–28, 11:40, 12:14–15, 12:41. Indeed, Perego discloses that "[s]ignaling over point-to-point links 320a–320n *or alternatively*, over bussed topologies, may incorporate different modulation methods." *Id.* at 8:42–47 (emphasis added). Perego goes on to explain the difference between a "point-to-point link" and a bus. *Id.* at 8:51–65. Thus, Perego discloses busses as an alternative to the point-to-point topology that Dr. Przybylski says is indicative of Rambus XDR.

Data width is another indicator that Perego is not limited to a Rambus architecture. Dr. Przybylski relies on Exhibit 2009 to explain Rambus XDR technology. *See* Ex. 2024 ¶ 99 (citing Exhibit 2009 to explain that "point-to-point" refers to Rambus XDR). The largest module data width disclosed in that exhibit is 36 bits. Ex. 2009, 10 (disclosing a 32-bit module data

width, which may be 36 bits wide with ECC). Perego, however, discloses a module data width of up to 128 bits (Ex. 1071, 14:16–23), which is further evidence that Perego's disclosure encompasses more than just Rambus XDR.

Perego also discloses that the buffer can be configured with a data width of 64 bits. Ex. 1071, 14:19–23 ("In an embodiment of the present invention, interface 596 includes 128 pins of which selectable subsets of 1, 2, 4, 8, 16, 32, 64 or all 128 pins (W_{DP}) may be used in order to configure the width of configurable width buffer device 391."). Petitioner asserts, with supporting testimony from Dr. Wolfe, that a person of ordinary skill in the art "would have understood that a data width of W_{DP}=64 corresponds to the 64-bit data width of a JEDEC-compliant registered DIMM module." Pet. 39 (citing Ex. 1003 ¶ 215; Ex. 1062, 5); *see* Ex. 1062 (Jan. 2002 JESD21-C RDIMM Specification), 5 (providing DIMM organization of "x72 ECC, x64").

Dr. Przybylski's testimony confirms that a 64-bit width was a JEDEC width. For example, Dr. Przybylski testifies that a person of ordinary skill in the art "would recognize the x64 and x72-wide memory modules mentioned in the '417 Patent, 2:47–53, as referencing JEDEC-standard compliant memory modules." Ex. 2024 ¶ 72 (citing Ex. 1066, 4). Dr. Przybylski also testifies that a person of ordinary skill in the art would have understood that, as of January 2005, a "disclosed DIMM module has a 64-bit data bus, just as all the JEDEC-standardized SDRAM-based DIMMs of the day." *Id.* ¶ 85.

Thus, the evidence shows that a 64-bit data width is a JEDEC-compliant module width and is not limited to a Rambus XDR module width, supporting Petitioner's contention that Perego's disclosure suggests a

module that can be configured to have a JEDEC interface. *See* Pet. 38. We do not agree with Patent Owner's suggestion that Perego's configurable buffer width makes it unsuitable to be implemented as an RDIMM, which has a fixed buffer width. *See* PO Resp. 23 ("Furthermore, the RDIMM relied on by Petitioners has a fixed buffer width (EX2003, 43:12–20; EX1064, 1–6, EX2024, ¶ 24), whereas configurable width buffer devices are central to Perego." (citing Ex. 1071, Abstract, Title, Figs. 3C, 4A, 5A, 5B, 13:6–17, 13:49–59, 14:52–15:6, 15:31–45, 17:22–33). We see no incompatibility where Perego discloses the RDIMM width along with other widths.

Petitioner also relies on Perego's disclosure of using individual control lines. Pet. 41 (citing Ex. 1071, 9:43–45, 9:58–60). Perego discloses an alternative to a packetized signaling approach in which "control lines (RQ) may comprise individual control lines, for example, row address strobe, column address strobe, etc., and address lines." Ex. 1071, 9:50–60. Petitioner argues that individual control lines are indicative of a JEDEC-style memory bus. Pet. Reply 6–7 (citing Ex. 1071, 9:58–60, 10:54–59, Fig. 4A; Ex. 1064, 6; Ex. 2025, 3; Ex. 1003 ¶¶ 217–218; Ex. 2033, 141:6–145:24, 148:18–149:6).

Patent Owner counters that, "[e]ven when Perego discusses providing 'individual control lines,' it never mentions a chip-select signal line (or any of the other signal lines characteristic of a JEDEC-style RDIMM, such as CKE, DQS, etc.)." PO Resp. 22 (citing Ex. 1071, 9:58–60; Ex. 2024 ¶¶ 129, 139; Ex. 1066, 6; Ex. 1069, 12; Ex. 2001, 20–23). Although this passage of Perego does not mention chip select signals, it mentions "row address strobe, column address strobe, etc., and address lines" as exemplary individual

control lines. Ex. 1071, 9:58–60. The evidence shows that row address strobe (RAS) and column address strobe (CAS) are JEDEC module input signals and not Rambus signals. Ex. 1066, 6 (RDIMM pins for RAS and CAS); Ex. 1062, 6 (same); Ex. 1095, 235:1–236:25 (Dr. Przybylski's testimony in which he agrees that a Rambus direct DRAM does not have pins for RAS and CAS signals as in DDR devices).

Dr. Przybylski also testifies that

> [a]nother of the essential aspects of Direct RDRAMs that differentiate them from all of the JEDEC-defined SDRAMs is the encoding of the 8-bit RQ control bus. Instead of presenting the entire command and address at once on 24 signal lines, captured by a single clock edge, the Direct RDRAM RQ bus has only 8 transmission lines. In addition, instead of 1 command spread across 24 signal lines, row commands with their row addresses are gathered into a packet and sent over 8 bit periods on only 3 lines. Column commands are sent with the column addresses, data masking and precharge indicators over 5 metal traces in the same 8 bit period.

Ex. 2024 ¶ 46. This testimony shows that individual address lines as disclosed in Perego are not characteristic of Rambus-type memories. Thus, contrary to Patent Owner's argument above, Perego expressly discloses "signal lines characteristic of a JEDEC-style RDIMM." *See* PO Resp. 22.

Patent Owner also argues that Perego's disclosure of individual lines "relates to secondary channel signal lines," i.e., those between the buffer and the memory devices, and not the primary channel between the memory controller and the memory module. PO Sur-reply 9 (citing Ex. 1071, 9:43–60). Perego's disclosure of using "individual control lines" appears in a discussion of Figure 4A (reproduced above in § II.D.2.a), in which Perego discloses that "[s]ignal lines of channels 415a and 415b include control lines (RQ), data lines (DQ) and clock lines (CFM, CTM)." Ex. 1071, 9:43–45.

Channels 415a and 415b are the channels between the buffer and the memory devices, so Perego's disclosure of individual lines certainly pertains to the secondary channels, as asserted by Patent Owner. Figure 4A, however, shows that the primary channel has the same signals lines—RQ, DQ, CTM, and CFM (shown vertically). In view of Perego's other disclosures suggesting non-Rambus module interfaces, discussed above, we do not understand Perego's disclosure that "control lines (RQ) may comprise individual control lines, for example, row address strobe, column address strobe, etc., and address lines" to be limited only to the RQ lines between the buffer and the memory devices. Rather, we find that this disclosure, read in light of Perego as a whole, at least suggests individual control lines on the primary channel as well.

Furthermore, other evidence also suggests that Perego is not limited to a Rambus-style architecture at the module interface. For example, Perego discloses that "the buffer device may be a configurable width buffer device to provide upgrade flexibility and/or provide high bandwidth among a variety of *possible module configurations* in the system." Ex. 1071, 3:25–28 (emphasis added). This indicates that Perego's disclosure is concerned with more than just one type of memory module, such as a Rambus module.

Perego further discloses that its buffered module provides flexibility because "new generations of controllers may be phased in which exploit features of new generations of memory devices while retaining backward compatibility with existing generations of memory devices." Ex. 1071, 6:34–43. In this context, it makes sense that Perego would leave the option open to use a bus on the interface between the module and the controller and not be limited to a point-to-point system, which would limit the ability to

interface with a system that uses a bus, such as a JEDEC system. Indeed, Perego states:

> However, using conventional signaling schemes, the bussed approaches lend efficiency towards resource utilization of a system and permits module interfacing for upgradeability.
>
> There is a need for memory system architectures or interconnect topologies that provide flexible and cost effective upgrade capabilities while providing high bandwidth to keep pace with microprocessor operating frequencies.

Id. at 2:22–29. Thus, Perego discloses that upgradeability was a goal and that busses permit such action.

Based on the foregoing discussion, we find that Perego's disclosure suggests a JEDEC-compliant interface to a memory controller. Furthermore, the evidence shows that JEDEC-compliant modules were dominant in the market at the relevant time. For example, Dr. Przybylski testifies that,

> in the 2004-2005 timeframe, the vast majority of the DRAM devices and modules sold would have been compliant with one of the JEDEC standards, such that a general reference to DRAM, especially in the context of usage main memory of general purpose computer and server systems, would suggest to a [person of ordinary skill in the art] the use of JEDEC-standard compliant SDRAM devices or modules.

Ex. 2024 ¶ 72. Petitioner asserts that the dominance of JEDEC-compliant modules "provid[es] additional motivation for the proposed combination." Pet. Reply 5–6. Patent Owner counters that the "mere fact that JEDEC-standardized modules dominated the market at the time of the invention also does not provide motivation to modify Perego." PO Sur-reply 11 (citing *Virtek Vision Int'l ULC v. Assembly Guidance Sys., Inc.*, 97 F.4th 882 (Fed. Cir. 2024). We agree with Petitioner on this point. In the case relied on by

Patent Owner, the Federal Circuit stated that "*KSR* did not do away with the requirement that there must exist a motivation to combine various prior art references in order for a skilled artisan to make the claimed invention," and the court reversed the Board's conclusion of obviousness finding that there was "no evidence of a design need or market pressure." *Virtek*, 97 F.4th at 887–88. Here, Patent Owner's own expert explains that JEDEC was a driving market force at the relevant time.

Patent Owner also argues that modification of Perego's architecture and memory system with a JEDEC-compatible bus would make it non-function. PO Resp. 29–30, 23–24 ("JEDEC-complaint, chip-select-dependent RDIMM architecture defined in JESD21-C is fundamentally at odds with the Rambus point-to-point topology and variable bit width interfaces of Perego."). But Patent Owner's "proposed" modifications would make Perego's system non-functional for Rambus, not for JEDEC, which was the dominant memory module style in the market. Given JEDEC as the standard, an ordinarily skilled artisan would have reason to pursue such a known option.

Patent Owner also argues that "Perego contrasts its memory modules with 'conventional DIMM module designs.'" PO Resp. 23–24 (quoting Ex. 1071, 6:27–33; citing Ex. 1071, 1:31–49, 2:15–30). Perego, however, draws a distinction based on the lack of buffered data lines in a conventional DIMM:

> In this embodiment, memory subsystems 330a-330n are buffered modules. By way of comparison, buffers disposed on the conventional DIMM module in U.S. Pat. No. 5,513,135 are employed to buffer or register control signals such as RAS, and CAS, etc., and address signals. Data I/Os of the memory devices disposed on the DIMM are connected directly to the DIMM

> connector (and ultimately to data lines on an external bus when the DIMM is employed in memory system 100).

Ex. 1071, 6:25–33. This passage shows that Perego discloses data buffering on the memory module, which was not present in DIMMs of that time. *See* Ex. 2024 ¶ 32 ("The two most common styles of JEDEC-standardized modules are called Unbuffered DIMMs (or UDIMMS), which contain principally just SDRAMs, and Registered DIMMs, which also include a register device for buffering the address and command buses (but not the data bus)."). We do not read Perego's disclosure of the lack of data buffering on DIMMs of the time as discounting all DIMM teachings. We find that Perego suggests a JEDEC-compliant interface with its disclosure of a 64-bit module width, and we further find that a person of ordinary skill in the art would have been motivated to make a module JEDEC-compliant based on JEDEC's dominance in the market at the time. *See* Ex. 1003 ¶ 188 (Dr. Wolfe's testimony that a person of ordinary skill in the art "would have been motivated to implement Perego's memory modules in a registered DIMM format that fits into the DIMM connectors of the time and uses the input and output signals of a DIMM module according to the relevant JEDEC standards, including JESD21-C.").

Patent Owner also argues that Petitioner's reliance on JESD21-C (Exs. 1062, 1066) for details of a JEDEC-compliant memory module is improper because JESD21-C is not part of any challenge in the Petition. PO Resp. 25–26. Rather, Patent Owner notes, JESD79-2 is the relied-upon JEDEC standards reference, and it relates to memory devices, not memory modules. *Id.* at 1, 20. So Patent Owner argues that the asserted combination of references does not teach unrecited "input chip select signals," which are inputs to the module, not to individual memory devices. *Id.* at 31.

We see no impropriety in Petitioner's reference to JESD21-C as support for the type of knowledge that the parties agree that a person of ordinary skill in the art would have had. *See* Pet. 9 (asserting that a person of ordinary skill in the art "would have been knowledgeable about the JEDEC DDR and DDR2 SDRAM standards used to standardize the functioning of memory devices, and the JEDEC 21-C standard"); PO Resp. 8 (asserting that a person of ordinary skill in the art would have been "knowledgeable about the operation of *standardized* DRAM and SDRAM memory devices and memory modules" (emphasis added)); *Id.* at 42–43 (arguing what a person of ordinary skill in the art would have understood "based on knowledge of the art and contemporaneous JEDEC standards"); Ex. 2024 ¶ 72 ("Dr. Przybylski "not[ing] that in the 2004–2005 timeframe, the vast majority of the DRAM devices and modules sold would have been compliant with one of the JEDEC standards, such that a general reference to DRAM, especially in the context of usage main memory of general purpose computer and server systems, would suggest to a [person of ordinary skill in the art] the use of JEDEC-standard compliant SDRAM devices or modules").

As discussed above, we find that Perego suggests a JEDEC-compliant interface with its disclosure of a 64-bit module width and that a person of ordinary skill in the art would have been motivated to make a module JEDEC-compliant based on JEDEC's dominance in the market at the time. Once a module is JEDEC-compliant, a person of ordinary skill in the art would have known that it would be configurable to receive a plurality of input chip select signals, which would be sent by a separate memory controller that is not claimed, based on the knowledge of JEDEC standards,

including JESD21-C. *See* Ex. 1062, 6 (identifying "SDRAM chip select lines" for DIMMs), *cited in* Pet. 57–58.

Furthermore, Patent Owner argues that "[c]hip-select signals are used to select ranks." PO Resp. 22–24 (citing Ex. 2031, 7 ("Rank: any DRAMs connected to the same CS")). Exhibit 2031's header ("JEDEC Standard No. 21-C") indicates that the exhibit pertains to JESD21-C, which is the module standard, and the exhibit states that it "describes the serial presence detects for the DDR2 version of the synchronous DRAM *modules*." Ex. 2031, 1 (emphasis added). The page cited by Patent Owner pertains to a field that "describes the number of ranks (Rank: any DRAMs connected to same physical CS) and package on the SDRAM module, and module height." *Id.* at 7. As Petitioner points out, JESDS79-2 discloses that "Chip Select . . . provides for external Rank selection on systems with multiple Ranks" and that chip select "is considered part of the command code." Ex. 1064, 6; *see* Pet. Reply 4–5. Thus, JESD79-2, which is part of the asserted grounds, discloses that chip select signals are received at the module for "external Rank selection" consistent with Patent Owner's cited evidence, which pertains to the module.

We further note that claim 1 is an apparatus claim, and "apparatus claims cover what a device *is*, not what a device *does*." *Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909 F.2d 1464, 1468 (Fed. Cir. 1990). Claim 1's recitation of "the second control signals being different from the first control signals" is a limitation pertaining to the claimed "logic," which is configured to provide the control signals. On this record, we find that Perego discloses logic that is configured to produce different control signals at least based on whether the operation is a read or a write.

Accordingly, based on the entire trial record, we agree with Petitioner's analysis and we credit Dr. Wolfe's testimony supporting Petitioner's position. Accordingly, we find that Perego discloses the "logic" limitation of claim 1.

3. Analysis of Dependent Claims 9–11, 23

Claim 9 depends from claim 1 and recites "wherein the first memory command includes at least one first chip select signal and the second memory command includes at least one second chip select signal."

Claim 10 depends from claim 9 and recites:

> wherein the memory module produces at least third and fourth chip select signals in response to the first memory command, the third chip select signal being provided to the at least one first memory integrated circuit and having an active value to cause the at least one first memory integrated circuit to receive or output data signals in response to the first memory command, the fourth chip-select signal being provided to the at least one second memory integrated circuit and having a non-active value to keep the at least one second memory integrated circuit from receiving or outputting data signals in response to the first memory command.

Claim 11 depends from 10 and recites:

> wherein the memory module produces at least fifth and sixth chip select signals in response to the second memory command, the fifth chip select signal being provided to the at least one first memory integrated circuit and having a nonactive value to keep the at least one first memory integrated circuit from receiving or outputting data signals in response to the first [sic: second] memory command, the sixth chip select signal being provided to the at least one second memory integrated circuit and having an active value to cause the at least one second memory integrated circuit to receive or output data signals in response to the second memory command.

Claim 23 depends from 21 and recites:

> wherein the first set of input command and address signals include at least one input chip-select signal, the method further comprising generating a first chip select signal and a second chip select signal in response to the first set of input command and address signals, the first chip-select signal being provided to the at least one first memory integrated circuit and having an active value to cause the at least one first memory integrated circuit to receive or output data signals in response to the first memory command, the second chip-select signal being provided to the at least one second memory integrated circuit and having a non-active value to keep the at least one second memory integrated circuit from receiving or outputting data signals in response to the first memory command.

Petitioner contends that the chip-select signals equate to the JEDEC standard for write and read command. Pet. 96 (citing Ex. 1064, 6, 37–46). Patent Owner argues, however, that because Perego uses Rambus module interfaces and because JESD79-2 relates to DDR2 SDRAM memory devices on the opposite side of the buffer from the module's bus or primary channel, "it is no surprise that neither reference discloses the '215 Patent's claimed input chip-select signals (Claims 9–11, 23)." PO Resp. 31 (citing Ex. 2033, 150:9–14 ("Rambus protocols at that time did not include distinct chip select wires, as far as I know."). Patent Owner notes that the Board preliminarily relied on a disclosure indicating that "chip-select information" is used in the "Rambus bus organization." *Id.* (citing Inst. Dec. 14–15 (quoting Ex. 1069, 11, 12). But then Patent Owner argues that "chip-select information" as used by Jacobs is not germane to the chip-select signals or lines required by JEDEC standards and the '417 Patent. *Id.* (citing Ex. 2024 ¶ 47).

For all the reason discussed previously, *see* Section II.D.2.g.2, we find that the combined teachings of Perego and JESD79-2 teach the use of chip-select signals as required by the challenged claims.

4. Analysis of Dependent Claims 8, 17, and 20

Claim 8 depends from claim 1 and recites "wherein the buffer comprises combinatorial logic, registers, and logic pipelines, and is configured to register an additional clock cycle for transferring the first data burst or the second data burst through the buffer." Claim 17 depends from claim 16 and recites "wherein the buffer comprises combinatorial logic, registers, and logic pipelines and is configured to register an additional clock cycle for transferring the first data burst through the buffer." Claim 20 depends from claim 19 and recites "wherein the buffer comprises combinatorial logic, registers, and logic pipelines and is configured to register an additional clock cycle for transferring the second data burst through the buffer."

Petitioner cites Perego's disclosure of a "scheme that could potentially route any single data bit signal to any data pair line or to any of the interface 596 data connections" (Ex. 1071, 18:49–54), and Petitioner argues that a person of ordinary skill in the art would have understood that such routing would "include '*logic pipelines*' to enable the '*data transfers*' through the '*circuitry*,' all in response to control signals that enable the data transfer." Pet. 95–96 (citing Ex. 1064, 23–25, 49; Ex. 1071, 13:49–59, 17:22–18:9, 18:48–54, Figs. 5B, 5C; Ex. 1003 ¶¶ 407–415). According to Petitioner, this is because the JEDEC standards specify that a read or write operation includes at least two steps: a Bank Activate command (with bank and row addresses), and then a Read or Write command (with bank and column addresses) followed by the actual transfer of data with pre-defined latencies, *id.* (citing Ex. 1064, 23, 24–25, 49; Ex. 1003 ¶¶ 415, 418). Petitioner further argues that "if ***any*** signal is registered on a memory

module — including data signals as in Perego — it was obvious to delay the signal for one full clock cycle to allow enough time for the functions of the register." Pet. Reply 17–18 (citing Pet. 81–83, 86–87, 119–121). Indeed, Petitioner asserts that "Netlist's expert admitted that putting a buffer on the data path would result in 'some delay,' and '[t]here are many examples of a register or buffer that includes ***a cycle*** of delay.'" *Id.* (citing Ex. 1095, 132:20–135:17; Ex. 2033, 100:15–103:10 ("When you register . . . you are necessarily delaying")) (alternation in original).

Patent Owner argues that the citations regarding delay due to registering the address and command signals are not relevant to the claim limitation. PO Resp. 36; PO Sur-reply 16–17. Patent Owner also argues that Additive Latency (AL) relates to concepts found in the DDR2 SDRAM standard but and not to any additional latency at the module level. *Id.* (citing Ex. 2024; Ex. 1064, 14). Patent Owner then asserts that Petitioner presents new arguments in its Reply. PO Sur-reply 18–19.

We do not agree with Patent Owner. Rather, for all the reason discussed previously, *see* Section II.D.2.g.2, we find that the combined teachings of Perego and JESD79-2 teach the use of routing through buffer using logic pipelines to register an additional clock cycle to enable the data transfers through the buffer as required by the challenged claims. Additionally, we find Petitioner's arguments to be properly responsive to Patent Owner's contentions presented in the Patent Owner's Response.

5. Dependent Claims 4, 25

Claim 4 depends from claim 1 and recites "further comprising an SPD device that reports an overall CAS latency of the memory module to the memory controller, the overall CAS latency having one more clock cycle

than an actual operational CAS latency of each of the plurality of memory integrated circuits." Claim 25 depends from claim 21 and recites "further comprising reporting an overall CAS latency of the memory module to the memory controller, the overall CAS latency having one more clock cycle than an actual operational CAS latency of the memory integrated circuits."

Petitioner argues that JEDEC-compliant memory modules include serial presence detect (SPD) that provide an overall CAS latency during initialization. Pet. 83 (citing Ex. 1071, 12:20–34, 15:52–53, 16:1–5; Ex. 1062, 68; Ex. 1003 ¶¶ 354–358); *see* Ex. 1071, 12:20–23 ("A serial interface 574 may be employed to couple signals utilized in initialization of module or memory device identification values, test function, set/reset, *access latency values*, vendor specific functions or calibration." (emphasis added)).

Patent Owner disputes Petitioner's contentions regarding the overall CAS latency for similar reasons as those proffered for claims 8, 17, and 20. PO Resp. 38. We find Petitioner's contentions persuasive.

First, Perego discloses that "buffer device 350 transceives and provides isolation between signals interfacing to controller 310 and signals interfacing to the plurality of memory devices 360." Ex. 1071, 6:12–15. This is similar to the '417 patent's disclosure "to add a buffer which electrically isolates the ranks of memory devices 30 from the memory controller 20." Ex. 1058, 22:46–49. Thus, Perego expressly discloses buffering data and its benefit—isolating the memory devices from the memory controller.

Second, the evidence shows that there would be some delay with a data buffer. *See* Ex. 1095, 132:20–133:6 (Dr. Przybylski's testimony that,

with a buffer on the data line of a memory module, "[i]nevitably, there's some delay, depending on the type of buffer and its characteristics internally").

Third, a person of ordinary skill in the art would have understood that CAS latency is measured in clock cycles. *See* Ex. 1095, 251:20–252:7 (Dr. Przybylski's testimony, referring to Exhibit 1064, that "[in DDR2, the latency is measured in clock cycles").

Accordingly, based on the entirety of the trial record, we agree with Petitioner and find that Perego teaches the coupled circuitry and reporting the CAS latency as recited by the challenged claim.

6. Dependent Claims 14, 15, and 26

Claim 14 depends from claim 1 and recites "wherein the buffer includes circuit components configurable to provide a first data path or a second data path depending on whether the first rank or the second rank is selected to communicate data with the memory controller." Claim 15 depends from claim 14 and recites "the at least one of the circuit components is configured to provide the first data path in response to the first control signals, and is configured to provide the second data path in response to the second control signals." Claim 26 depends from claim 21 and recites "wherein the buffer includes circuit components configurable to provide a first data path or a second data path depending on whether the first rank or the second rank is caused to communicate data with the memory controller."

Petitioner argues that Perego discloses data paths "for selectively coupling the memory bus, on one hand, to the rank of memory devices targeted by the buffer device for a read or write command, on the other

hand," and Petitioner refers to its contentions for relevant limitations of claim 1. Pet. 108–110 (citing Ex. 1003 ¶¶ 483–488).

Patent Owner contends, however, that a person of ordinary skill in the art would have understood "the interfaces 520a and 520b of configurable width buffer device 391 are part of a pair working in tandem, controlled by the Request and Address Logic 540," and in a DDR SDRAM configuration, they would all be part of a single rank. PO Resp. 39 (citing Ex. 2024 ¶ 164). Thus, Patent Owner argues that there are no "first rank" and "second rank" or "first data path" and "second data path" as required by these claims. *Id.* (citing Ex. 2024 ¶ 190).

We agree with Petitioner's contentions for the same reasons discussed above regarding claim 1 and the combine teachings of Perego and JESD79-2. Accordingly, based on the entirety of the trial record, we agree with Petitioner and find that Perego teaches the coupled data pathway as recited by the challenged claim.

7. Claims 2, 3, 5–7, 10, 12, 13, 16, 18, 19, 21, 22, 24, 27–29

Other than its arguments for independent claim 1, which we address above in § II.D.2, Patent Owner does not raise additional arguments for these claims. Nonetheless, the burden remains on Petitioner to demonstrate unpatentability. *See Dynamic Drinkware*, 800 F.3d at 1378. We have reviewed Petitioner's arguments and evidence, summarized above, and we find them persuasive. Therefore, having considered the full record developed during the trial, we conclude that claims 2, 3, 5–7, 10, 12, 13, 16, 18, 19, 21, 22, 24, 27–29 are unpatentable as having been obvious over the combined teachings of Perego and JESD79-2.

3. Objective indicia of non-obviousness

Patent Owner does not present objective evidence of non-obviousness other than to respond to Petitioner's assertion of evidence of "simultaneous invention." PO Resp. 55–56. As discussed, the combination of Perego and JESD79-2 teaches or renders obvious all of the limitations of claim 1, and there is no objective evidence of non-obviousness in the record.

4. Conclusion for the Perego and JESD79-2 Challenge

We have considered the full trial record, and, for the reasons discussed above and based on Petitioner's contentions and evidence, we conclude that claims 1–29 would have been obvious to a person of ordinary skill in the art based on the combined teachings of Perego and JESD79-2.

E. Remaining Challenges

Because we determine that all challenged claims are unpatentable as discussed above, we need not separately assess the challenges to patentability based on the combinations of (1) Perego, JESD79-2, and Ellsberry, (2) Perego, JESD79-2, and Halbert, and (3) Perego, JESD79-2, and Matsui. 35 U.S.C. § 318(a) ("If an inter partes review is instituted and not dismissed under this chapter, the Patent Trial and Appeal Board shall issue a final written decision with respect to the patentability of any patent claim challenged by the petitioner and any new claim added under section 316(d)."); *Bos. Sci. Scimed, Inc. v. Cook Grp. Inc.*, 809 F. App'x 984, 990 (Fed. Cir. 2020) (nonprecedential) ("We agree that the Board need not address issues that are not necessary to the resolution of the proceeding.").

III. PETITIONER'S MOTION TO EXCLUDE

Petitioner filed a Motion to Exclude Exhibit 2010 and portions of Exhibit 2003. Paper 35. Patent Owner relies on Exhibit 2010 to challenge Petitioner's combination of Perego and Ellsberry. PO Resp. 51–52; PO Sur-reply 23. We do not reach this ground and, therefore, do not rely on Exhibit 2010 in a manner adverse to Petitioner. We have considered the cited portions of Exhibit 2003 in our analysis above and do not rely on this testimony in a manner adverse to Petitioner.

Therefore, we dismiss the Motion to Exclude as moot.

IV. CONCLUSION[9]

For the reasons discussed above, we determine that Petitioner has proven, by a preponderance of the evidence, that claims 1–29 of the '215 patent are unpatentable, as summarized in the following table:

Claim(s)	35 U.S.C. §	Reference(s)/Basis	Claims Shown Unpatentable	Claims Not Shown Unpatentable
1–29	103(a)	Perego, JESD79-2	1–29	
1–29	103(a)	Perego, JESD79-2, Ellsberry[10]		
1–29	103(a)	Perego, JESD79-2, Halbert		
1–29	103(a)	Perego, JESD79-2, Matsui		
Overall Outcome			1–29	

[9] Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner's attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. *See* 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. *See* 37 C.F.R. § 42.8(a)(3), (b)(2).

[10] As explained above, because we determine that the challenged claims are unpatentable based on the combination of Perego and JESD79-2, we decline to address the remaining grounds.

V. ORDER

Accordingly, it is

ORDERED that claims 1–29 of the '215 patent have been shown to be unpatentable;

FURTHER ORDERED that Petitioner's Motion to Exclude (Paper 35) is *dismissed*; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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